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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,590	03/01/2004	Todd P. Lukanc	H1775	9600
45305	7590	04/21/2006	EXAMINER	
RENNER, OTTO, BOISSELLE & SKLAR, LLP (AMDS)			TO, TUYEN P	
1621 EUCLID AVE - 19TH FLOOR			ART UNIT	
CLEVELAND, OH 44115-2191			PAPER NUMBER	
			2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

N/A

Office Action Summary	Application No. 10/790,590	Applicant(s) LUKANC ET AL.	
	Examiner Tuyen To	Art Unit 2825	<u>TT</u>

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 March 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-31 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-31 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 March 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>07/01/2004</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This is a response to the communication filed on 03/01/2004. Claims 1-31 are pending.

Specification

1. The abstract of the disclosure is objected to because it includes the title. The title should be removed from the abstract (page 22). Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-9, 12-18, 20-24, and 26-31** are rejected under 35 U.S.C. 102(e) as being anticipated by White et al. (US Pub. No.2003/0229868).

Claim 1, White et al. disclose a method of designing an integrated circuit (IC) device having desired electrical characteristics, said method comprising:

- providing an initial IC device design (Fig.2, element 36, paragraph [0118]);
- generating a layout representation corresponding to the initial IC device design (Fig.2, element 36, paragraph [0118] ; Figs. 10A-10C; paragraph[0144]);
- simulating how structures within the layout representation will pattern on a wafer (Figs. 10B-10C; paragraph[0144]);
- based on the simulating step, determining whether actual electrical characteristics associated with the initial IC device design sufficiently match the desired electrical characteristics (paragraph[0144]); and
- if the actual electrical characteristics associated with the initial IC device design do not sufficiently match the desired electrical characteristics, modifying the initial IC device design (Figs. 10B-10C; paragraphs[0144], [0006], [0014], and [0141]).

Claim 2, White et al. disclose the method of claim 1, wherein the step of determining whether the actual electrical characteristics associated with the initial IC device design sufficiently match the desired electrical characteristics includes:

- determining actual dimensions of structures within the layout representation based on the simulating step (paragraph[0112]-[0114]; [0135]); and
- determining the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation (paragraph[0138] and [0144]).

Claim 3, White et al. disclose the method of claim 2, wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using a look-up table (Fig. 25; paragraph [0211]).

Claim 4, White et al. disclose the method of claim 2, wherein the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation are determined using an electrical modeling program in which the actual dimensions of the structures are input (paragraphs [0047], [0140], and [0147]).

Claim 5, White et al. disclose the method of claim 1, wherein the desired electrical characteristics include at least one of drive current, gain and switching speed (paragraphs[0006] and [0201]).

Claim 6, White et al. disclose the method of claim 1, wherein the step of generating a layout representation corresponding to the initial IC device design includes minimizing the scale of the layout representation (paragraph[0009]).

Claim 7, White et al. disclose the method of claim 1, wherein the initial IC device design includes a desired relationship between at least two structures within the IC device design (paragraph[0115]).

Claim 8, White et al. disclose the method of claim 7, further comprising:
determining an amount of process-related variation associated with at least two structures within the Layout representation of the IC device design (paragraphs[0112]-[0115]).

Claim 9, White et al. disclose the method of claim 8, wherein determining an amount of process-related variation associated with at least two structures within the Layout representation includes:

simulating how structures within the layout representation will pattern on a wafer (paragraphs[0135]-[0138]); and

measuring a feature of the simulated structures, said feature being indicative of process-related variation (paragraphs[0135]-[0138]).

Claim 12, White et al. disclose the method of claim 9, said method further comprising:

measuring the feature indicative of process-related variation for one or more simulated structures over a process window of focus and intensity (Fig. 3; paragraphs[0120]-[0121] and Fig. 60A; paragraphs[0306]).

Claim 13, White et al. disclose the method of claim 12, wherein the simulated structures are at different locations within the layout representation (Fig. 42; paragraph [0255]).

Claim 14, White et al. disclose the method of claim 9, wherein simulating how structures within the layout representation will pattern on a wafer includes simulating how structures within the layout representation will pattern as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design (Fig. 25; paragraph[0211]; paragraph[0168]), (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC

device design, and (v) size of a structure with respect to other adjacent structures (Fig. 25; paragraph[0211]).

Claim 15, White et al. disclose the method of claim 9, further comprising:
determining whether at least a portion (paragraph[0009]) of the IC device design is optimized with respect to process-related variations (paragraph[0304]).

Claim 16, White et al. disclose the method of claim 15, further comprising:
if a portion of the IC device design is not optimized with respect to process-related variations, modifying at least a portion of the IC device design (paragraphs[0009],[0304], and [0135]) .

Claim 17, White et al. disclose the method of claim 16, wherein modifying at least a portion of the IC device design includes modifying at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design (paragraph [0142]), (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures (paragraph [0142]).

Claim18, White et al. disclose the method of claim 9, wherein the process-related variations include variations caused by at least one of (i) mask generation (pagraph[0112]), (ii) wafer patterning, (iii) pre-patterning processing, and (iv) post-patterning processing.

Claim 20, White et al. disclose an integrated circuit (IC) device designed by the method of claim 1 (paragraph [006]).

Claim 21, White et al. disclose a method of designing an integrated circuit (IC) device, said method comprising:

providing an initial IC device design (Fig.2, element 36, paragraph [0118]);
generating a layout representation corresponding to the initial IC device design (Fig.2, element 36, paragraph [0118] ; Figs. 10A-10C; paragraph[0144]); and
determining an amount of process-related variation in how at least a portion of the layout representation will pattern on a wafer (paragraph[0009], [0137], and[0144]).

Claim 22, White et al. disclose the method of claim 21, further comprising:
determining whether at least a portion of the IC device design is optimized with respect to process-related variations (paragraph[0009] and [0302]-[0304]); and
if a portion of the IC device design is not optimized with respect to process-related variations, modifying at least a portion of the IC device design (paragraphs [0009] , [0135], and [0144]) .

Claim 23, White et al. disclose the method of claim 22, wherein modifying at least a portion of the IC device design (paragraphs [0009], [0135], and [0144]) includes modifying at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design (paragraph [0142]), (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures.

Claim 24, White et al. disclose the method of claim 21, wherein determining an amount of process-related variation in how at least a portion of the Layout representation will pattern on a wafer includes:

simulating how structures within the layout representation will pattern on a wafer (paragraphs[0135]-[0138]); and

measuring a feature of the simulated structures, said feature being indicative of process-related variation (paragraphs[0135]-[0138]).

Claim 26, White et al. disclose the method of claim 24, said method further comprising:

measuring the feature indicative of process-related variation for one or more simulated structures over a process window of focus and intensity (Fig. 3; paragraphs[0120]-[0121] and Fig. 60A; paragraphs[0306]).

Claim 27, White et al. disclose the method of claim 26, wherein the simulated structures are at different locations within the layout representation (Fig. 42; paragraph[0255]).

Claim 28, White et al. disclose the method of claim 21, further comprising:

determining whether the layout representation will pattern as an IC device having desired electrical characteristics (Fig. 10B, paragraph[0144]).

Claim 29, White et al. disclose the method of claim 28, wherein determining whether the layout representation will pattern as an IC device having desired electrical characteristics includes:

simulating how structures within the layout representation will pattern on a

wafer (Figs. 10B-10C; paragraph[0144]); and

based on the simulating step, determining whether actual electrical characteristics associated with the initial IC device design sufficiently match the desired electrical characteristics (paragraph[0144]).

Claim 30, White et al. disclose the method of claim 29, wherein the step of determining whether the actual electrical characteristics associated with the initial IC device design sufficiently match the desired electrical characteristics includes:

determining actual dimensions of structures within the layout representation based on the simulating step (paragraph[0112]-[0114]; [0135]); and

determining the actual electrical characteristics associated with the actual dimensions of the structures within the layout representation (paragraph[0138] and [0144]).

Claim 31, White et al. disclose a computer-implemented method in which an initial integrated circuit (IC) device design is provided, said method comprising:

generating a layout representation corresponding to the initial IC device design (Fig.2, element 36, paragraph [0118] ; Figs. 10A-10C; paragraph[0144]);

simulating how structures within the Layout representation will pattern on a wafer (Figs. 10B-10C; paragraph[0144]);

based on the simulating step, determining an amount of process-related variation in how at least a portion of the layout representation will pattern on a wafer (paragraph[0009], [0137], and[0144]); and

determining whether the layout representation will pattern as an IC device

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having desired electrical characteristics (Fig. 10B, paragraph[0144]).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. **Claims 10-11, 19, and 25** are rejected under 35 U.S.C. 103(a) as being unpatentable over White et al. in view of Rosenbluth et al. (US Pub. No. 2002/0140920).

Claim 10 and similarly recited claim 25, White et al. disclose substantially all the elements in claims 10 and 25, *except* wherein the feature indicative of process-related variation is at least one of (i) slope of edge intensity and (ii) logarithm of slope of edge intensity.

Rosenbluth et al. disclose wherein the feature indicative of process-related variation is at least one of (i) slope of edge intensity (paragraphs [0015] and [0019]) and (ii) logarithm of slope of edge intensity (paragraph [0099]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the method of White et al. with the method disclosed by Rosenbluth et al. because such combined method includes slope of edge intensity / logarithm of slope of edge intensity would provide a technique for optimally choosing illumination distribution and mask features (paragraph[0021]).

Claim 11, the method of claim 10, wherein:

a larger slope of edge intensity or logarithm of slope of edge intensity is

indicative of a smaller process-related variation (Rosenbluth et al. , paragraphs[0019] and [0082]); and

a smaller slope of edge intensity or logarithm of slope of edge intensity is indicative of a larger process-related variation (Rosenbluth et al. , paragraphs[0019]and [0082]).

Claim 19, the method of claim 11, further comprising:

providing feedback to a designer regarding how a given structure will print on a wafer (White et al., paragraph [0224]) as a function of at least one of (i) proximity of a structure to other structures, (ii) density of structures within a portion of the IC device design, (iii) orientation of a structure, (iv) placement of a structure within a portion of the IC device design, and (v) size of a structure with respect to other adjacent structures (White et al., paragraphs [0115],[0178],[0220] and [0224]).


Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Tuyen To
Patent Examiner
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PAUL DINH
PRIMARY EXAMINER